RICHARD DORRANCE

+1 (619) 251-1871 | RDORRANCE@UCLA.EDU

WWW.RDORRANCE.BOL.UCLA.EDU

RESEARCH INTERESTS

My research interests cover a broad swath of engineering disciplines, including post-CMOS device development and integration; high-performance, energy-efficient computing architectures; neuromorphic engineering; and high-performance computing for bioinformatics. My dissertation work proposes an architecture for improving the energy-efficiency and performance of sparse linear algebra in SoCs that utilizes post-CMOS memory technologies.

EDUCATION

PH.D. ELECTRICAL ENGINEERING — EXPECTED 2015

University of California, Los Angeles

- Advisor: Dejan Marković
- Dissertation: An Energy-Efficient Sparse-BLAS Coprocessor using STT-MRAM

  Description: Proposes the integration of spintronic memories to create new architectures for high-performance data processing to address the issue of poor computational throughput of sparse linear algebra.

M.S. ELECTRICAL ENGINEERING — JUNE 2011

University of California, Los Angeles

- Advisor: Dejan Marković
- Thesis: Modeling and Design of STT-MRAMs

  Description: Proposes a comprehensive circuit-device co-design methodology for improved memory density and yield in STT-MRAM, and provides guidance on the future direction of MTJ device development and materials optimization.

B.S. ELECTRICAL ENGINEERING AND COMPUTER SCIENCES — MAY 2009

University of California, Berkeley

- Eta Kappa Nu (HKN) Activities Officer (Spring 2009)

HONORS AND AWARDS

2014 MEDIATEK FELLOWSHIP — FINALIST — **AUGUST 2014**

2013-2014 HENRY SAMUELI EXCELLENCE IN TEACHING AWARD — **JUNE 2014**

2014 QUALCOMM INNOVATION FELLOWSHIP — FINALIST — **DECEMBER 2013**

IEEE SOLID-STATE CIRCUITS SOCIETY STUDENT TRAVEL GRANT — **FEBRUARY 2013**

UNIVERSITY FELLOWSHIP, UCLA — **NOVEMBER 2012**

PUBLICATIONS

JOURNAL

[J5] H. Lee, **R. Dorrance**, S. Basir-Kazeruni, D. Marković, P.K. Amiri , and K.L. Wang, "A Spin-based Artificial Neuron for Ultra-Scale Neuromorphic Computing," *IEEE Trans. Nanotechnol. (**TNANO**), under review.*

[J4] **R. Dorrance** and D. Marković, "A Scalable Sparse Linear Algebra Kernel for Accelerating Bioinformatics on FPGAs," *IEEE/ACM Trans. Comput. Biol. Bioinf. (**CBB**), under review.*

[J3] H. Lee, J.G. Alzate, **R. Dorrance**, D. Marković, P.K. Amiri , and K.L. Wang, "Design of a Fast and Low-Power Sense Amplifier and Writing Circuit for High-Speed MRAM," *IEEE Trans. Magn. (**TMAG**), accepted.*

[J2] **R. Dorrance**, J.G. Alzate, S. Cherepov, P. Upadhyaya, I.N. Krivorotov, J.A. Katine, J. Langer, K.L. Wang, P.K. Amiri, and D. Marković, "A Diode-MTJ Crossbar Memory Cell Using Voltage-Induced Unipolar Switching for High-Density MRAM," *IEEE Electron Device Lett. (**EDL**)*, vol. 34, no. 6, pp. 753-755, Jun. 2013.

[J1] **R. Dorrance**, F. Ren, Y. Toriyama, A.A. Hafez, C.-K.K. Yang, D. Marković, "Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell for STT-RAM," *IEEE Trans. Electron Devices (**TED**)*, vol. 59, pp. 878-887, no. 4, Apr. 2012.

CONFERENCE

[C7] **R. Dorrance**, F. Ren, and D. Marković, "An Efficient Sparse Matrix-Vector Multiplication (SpMxV) Kernel for Sparse-BLAS on FPGAs," in *Proc. 2014 ACM/SIGDA Int. Symp. Field-Programmable Gate Arrays (**FPGA'14**)*, pp. 161-170, Feb. 2014.

[C6] F. Ren, **R. Dorrance**, W. Xu, and D. Marković, "A Single-Precision Compressive Sensing Signal Reconstruction Engine on Reconfigurable Platform," in *Proc. 23rd Int. Conf. on Field-Programmable Logic and Applications (**FPL'13**)*, pp. 1-4, Sep. 2013.

[C5] **R. Dorrance**, J.G. Alzate, S. Cherepov, P. Upadhyaya, K.L. Wang, P.K. Amiri, and D. Marković, "Voltage-Controlled MRAM for 3D Stackable Non-Volatile Memories," *IEEE Int. Solid-State Circuits Conference* Student Research Preview *(**ISSCC'13**)*, Feb. 2013.

[C4] J. G. Alzate, P.K. Amiri, P. Upadhyaya, S.S. Cherepov, J. Zhu, M. Lewis, **R. Dorrance**, J. A. Katine, J. Langer, K. Galatsis, D. Marković, I. Krivorotov, and K. L. Wang, "Voltage-Induced Switching of Nanoscale Magnetic Tunnel Junctions," in *Proc. Int. Electron Devices Meeting (**IEDM'12**)*, pp. 29.5.1-29.5.4, Dec. 2012.

[C3] F. Ren, H. Park, **R. Dorrance**, Y. Toriyama, A. Amin, C.-K.K. Yang, D. Marković, "A Body-Voltage-Sensing-Based Short Pulse Reading Circuit for Advanced Spin-Torque Transfer RAMs (STT-RAMs)," in *Proc. 13th Int. Symp. on Quality Electronic Design (**ISQED'12**)*, pp, 275 282, Mar. 2012.

[C2] H. Park, **R. Dorrance**, A. Amin, F. Ren, D. Marković, C.-K.K. Yang, "Analysis of STT-RAM Cell Design with Multiple MTJs Per Access," in *Proc. ACM/IEEE Int. Symp. on Nanoscale Arch. (**NANOARCH'11**)*, pp. 32-36, Jun. 2011.

[C1] **R. Dorrance**, F. Ren, Y. Toriyama, A. Amin, C.-K.K. Yang, D. Marković, "Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell," in *Proc. ACM/IEEE Int. Symp. on Nanoscale Arch. (**NANOARCH'11**)*, pp. 53-58, Jun. 2011.

PATENTS

[P3] P. K. Amiri, **R. Dorrance**, H. Lee, S. Basir-Kazeruni, D. Marković, K. L. Wang, "An Artificial Neuron based on the Spin Hall Effect," *US Patent*, University of California Case No. 2014-925-1, Nov. 2014.

[P2] P. K. Amiri, **R. Dorrance**, D. Marković, K. L. Wang, "Nonvolatile Magneto-Electric Random Access Memory Circuit with Burst Writing and Back-to-Back Reads," *US Patent*, US 20140071732 A1, Mar. 2014.

[P1] P. K. Amiri, **R. Dorrance**, D. Marković, K. L. Wang, "Read-Disturbance-Free Nonvolatile Content Addressable Memory (CAM)," *US Patent*, US 20140071728 A1, Mar. 2014.

INVITED TALKS

[T5] **R. Dorrance**, "An Energy-Efficient Sparse Linear Algebra Kernel for Bioinformatics and Health Monitoring on Mobile SoCs," in *2014 MediaTek Fellowship Finalist Presentations*, Los Angeles, California, Aug. 2014.

[T4] **R. Dorrance** and H. Lee, "An Ultra-Low-Power, High-Density Neural Network Based on the Spin-Hall Effect," in *2014 Qualcomm Innovation Fellowship Finalist Presentations*, Bridgewater, New Jersey, Mar. 2014.

[T3] **R. Dorrance** and D. Marković, "An Energy-Efficient Sparse Linear Algebra Kernel for High-Performance Computing in a Mobile Environment," in *UCLA Electrical Engineering Department Annual Research Review*, Los Angeles, California, Dec. 2013.

[T2] **R. Dorrance** and J.G. Alzate, "Magneroelectric Random Access Memory," in *UCLA Electrical Engineering Department Annual Research Review*, Los Angeles, California, Dec. 2012.

[T1] F. Ren and **R. Dorrance**, "Short Pulse Reading (SPR) for STT-RAMs," in *Western Institute of Nanoelectronics Annual Review*, Los Angeles, California, Oct. 2011.

TEACHING EXPERIENCE

Teaching at the University of California, Los Angeles

EEM216A: DESIGN OF VLSI CIRCUITS AND SYSTEMS **2012 – 2014**

Teaching Assistant/Lecturer

- Graduate-level course focusing on VLSI circuit and system design in state-of-the-art CMOS technologies.
- Lectured students on the design flow for VLSI circuit design using RTL: simulation, synthesis, place and route.
- Developed new labs to teach RTL design and synthesis for a revised course curriculum.
- Designed the course projects to emphasize finite state machine (FSM) design, circuit- and architecture-level optimizations, and layout in an advanced 28nm technology node:
  - Fall 2012: game display engine for an adventure game.
  - Winter 2014: game display engine for a PacMan-based game.
  - Fall 2014: 2D graphics engine for a 4-in-1 video game.
- Awarded the 2013-2014 Henry Samueli Excellence in Teaching Award from the UCLA Electrical Engineering Department.

EE215B: ADVANCED DIGITAL INTEGRATED CIRCUITS **WINTER 2013**

Teaching Assistant

- Graduate-level course focusing on modern logic families and memories for VLSI circuit and system design.
- Migrated course labs to a Synopsys 32/28nm Interoperable PDK.
- Designed the course project (a 1Mbit SRAM array with yield greater than 99.9%) to focusing on the core course concepts.

Teaching at the University of California, Berkeley

EE140: LINEAR INTEGRATED CIRCUITS **SPRING 2008**

Undergraduate Student Instructor

- Upper division analog circuits design course focusing on design and analysis of MOS and BJT amplifiers.
- Help designed and test a new set of labs and projects for a revised course curriculum.

RESEARCH EXPERIENCE

Research at the University of California, Los Angeles

HARDWARE-ACCELERATED RETINAL SPIKE SORTING **01/14 – PRESENT**

- Development of an FPGA system to accelerate the sorting and analysis of a 512-channel retinal electrode array in collaboration with Stanford.

ENERGY EFFICIENT SPARSE-BLAS KERNAL **06/12 – PRESENT**

- Development of a sparse-BLAS FPGA kernel with a 100-200x speedup over CPUs and 20-40x speedup over GPUs.
- Energy-efficiency improvement of 38-50x over state-of-the-art CPUs and GPUs.
- ASIC implementation planned in a 28nm technology node.

REAL-TIME 3-D TOMOGRAPHIC IMAGING WITH FPGAS **09/11 – 05/12**

- Research into and development of massively parallelized algorithms for filtered and iterative backprojection on FPGAs.
- Development of an end-to-end, FPGA-based system for high speed 3-D tomographic reconstructions.

NONVOLATILE LOGIC **09/10 – PRESENT**

- Research into and development of voltage-controlled MTJs for nonvolatile computing.
- Design, fabrication, and testing of MTJ-based memories and logic in a 65nm technology node.
- Development of an MTJ-based artificial neuron for Neuromorphic computing applications.

STT-MRAM **09/09 – 12/13**

- Research into and development of STT-based MTJs for next generation memory technologies in collaboration with the UC Irvine and the University of Minnesota.
- Development of a physics-based compact model for fast circuit-level simulations of MTJ devices (Verilog-A).
- Design, fabrication, and testing of MTJ-based memories in 90nm, 65nm, and 45nm technology nodes.

Industry Experience

GLOBALFOUNDRIES INC.: *SUNNYVALE, CA* **SUMMER 2013**

- Exploratory research into spintronic memory development. Scaling STT-RAM into a 22nm node.
- Development of STT-RAM architectures for eFLASH and L2/L3 Cache replacements.

IMEC: *LEUVEN, BELGIUM* **SPRING 2013**

- Design and development of a back-end-of-line STT-RAM process for 65nm CMOS.
- Design of a 1MB STT-RAM test chip for MTJ and RRAM device characterization.

SPAWAR SYSTEMS CENTER: *SAN DIEGO, CA* **SUMMER 2008**

- Research into spectral and temporal seismic wave patterns using NOAA costal hydrophones arrays.
- Design of algorithms for detecting, localizing, and classifying underwater seismic events.

MENTORING

GRADUATE MENTORING

- Mentored and advised 14 graduate students completing the project option for an M.S. degree at UCLA:
  - Summer 2012: Two students worked on extending and improving the accuracy of our MTJ compact model.
  - Spring 2013: Two students worked on accelerating 3D tomography on heterogeneous multi-core systems.
  - Summer/Fall 2013: Three students developed and optimized code for performing sparse linear algebra on heterogeneous multi-core systems.
  - Spring/Summer 2014: Four student implemented various architectures for performing CSR-based spare matrix-vector multiplication on FPGAs.
  - Summer/Fall 2014: Three students implemented several spike detection, alignment, and sorting algorithms on a GiDEL ProcStar IV FPGA development board.

UNDERGRADUATE MENTORING

- Mentored and advised four undergraduate students at UCLA:
  - Summer 2013: A student worked on benchmarking the reconstruction performance of various hardware configurations for 3D tomographic reconstructions.
  - Summer 2014: Two students developed a Simulink/Matlab testing environment for automated digital ASIC chip testing.
  - Summer/Fall 2014: A student developed a DDR2 memory controller for a Kintex-7 FPGA development board.

PROFESSIONAL ACTIVITIES

Professional Memberships

ASSOCIATION FOR COMPUTING MACHINERY **01/14 – PRESENT**

Non-profit Professional Association

- Current Status: Student Member

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS **09/09 – PRESENT**

Non-profit Professional Association

- Current Status: IEEE Student Member
- Active member of the IEEE Communications Society, IEEE Electron Devices Society, IEEE Magnetics Society, and IEEE Solid-State Circuits Society.

ETA KAPPA NU (HKN), MU CHAPTER **12/08 – PRESENT**

Electrical and Computer Engineering Honor Society

- Held position of Activities Officer during Spring 2009 semester (12/08 to 5/09).

Peer Review

INVITED REVIEWER FOR JOURNALS

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE Transactions on Electron Devices (TED)
- IEEE Electron Device Letters (EDL)

- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
- IEEE Transactions on Nanotechnology (TNANO)
- IEEE Transactions on Very Large Scale Integration Systems (VLSI)
- IEEE Transactions on Magnetics (TMAG)
- IEEE Design and Test of Computers
- SPIN

INVITED REVIEWER FOR CONFERENCES

- IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2014

REFERENCES

DR. DEJAN MARKOVIĆ

Professor, Electrical Engineering Department, UCLA
Co-Founder and Technical Advisor, Flex Logix Technologies, Inc.

- Office: 56-147E Engineering IV Building, Box 951594, Los Angeles, CA 90095-1594
- Email: dejan@ee.ucla.edu
- Phone: (310) 825-8656

DR. KANG L. WANG

Professor, Electrical Engineering Department, UCLA
Editor-in-Chief, IEEE Transactions on Nanotechnology (TNANO)

- Office: 66-147C Engineering IV Building, Box 951594, Los Angeles, CA 90095-1594
- Email: wang@ee.ucla.edu
- Phone: (310) 825-1609

DR. PEDRAM KHALILI-AMIRI

Professor, Electrical Engineering Department, UCLA
Co-Founder and CTO, Inston Inc.

- Office: 66-127G Engineering IV Building, Box 951594, Los Angeles, CA 90095-1594
- Email: pedramk@ucla.edu
- Phone: (310) 825-9095

DR. CHIH-KONG KEN YANG

Professor, Electrical Engineering Department, UCLA
Co-Founder and VP of Product Engineering, Pluribus Networks, Inc.

- Office: 56-147A Engineering IV Building, Box 951594, Los Angeles, CA 90095-1594
- Email: yang@ee.ucla.edu
- Phone: (310) 825-3665

DR. HAMID HATAMKHANI

Lecturer, Electrical Engineering Department, UCLA
Principal Scientist, Broadcom Corporation

- Office: 66-144 Engineering IV Building, Box 951594, Los Angeles, CA 90095-1594
- Email: hamidha@gmail.com
- Phone: (310) 206-4237